

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:

Masahiro Ishida, et al.

Serial No.:

09/699,077

Filing Date:

October 27, 2000

Title:

Method and Apparatus for Fault

Simulation of Semiconductor

Integrated Circuit

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Examiner: Ayal Sharon

Art Unit: 2123

APR 2 3 2004

April 19, 2004

Commissioner of Patents P.O. Box 1450 Alexandra, VA 22313-1450

Technology Center 2100

INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to the duty of disclosure set forth in 37 CFR § 1.56, Applicants respectfully submit the following information disclosure statement.

The undersigned certifies that each of the following references was contained in a communication in connection with a counterpart foreign application not more than three months prior to the filing of this statement.

The disclosed reference is:

EPO 0 878 761, European Patent Office, published November 18, 1998.

Applicants respectfully request that the Examiner initial the cited references shown on the enclosed form PTO-1449 and that the references be made of record in the present application.

Respectfully submitted,

David N. Lathrop

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Enc. US PTO Form 1449

Cited reference (1)
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Certificate of Mailing Under 37 CFR 1.8

I certify that this Information Disclosure Statement and all enclosed materials are being deposited with the United States

Postal Service on April 19, 2004 with sufficient postage as

first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450...

David N. Lathrop

Docket: KPO089

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U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

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INFORMATION DISCLOSURE STATEMENT
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APPLICANT
Masahiro Ishida, et al.

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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP; draw line through citation if not in conformance and not considered. Include copy of this form with next communication with applicant.